

Low Power 1-Bit ADC Array with Serial Output, Phase I

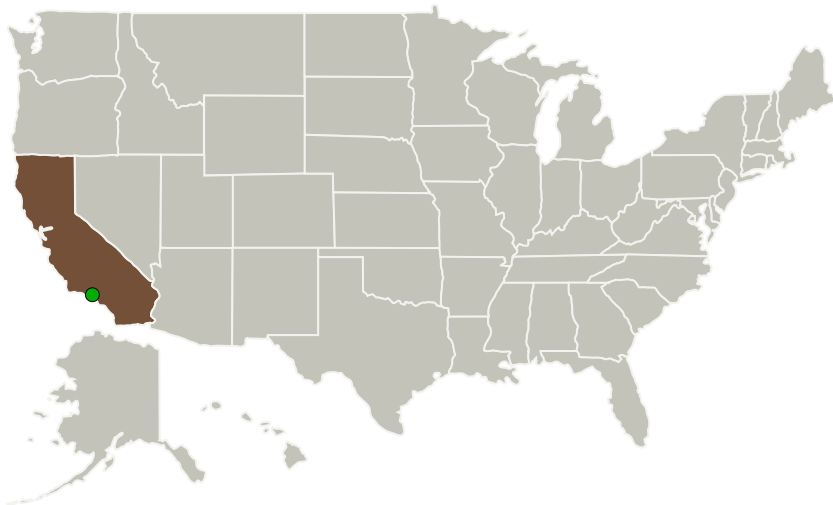
Completed Technology Project (2010 - 2010)



Project Introduction

Microwave interferometers for NASA missions such as PATH and SCLP consist of up to 900 receivers. Each receiver requires I and Q ADCs (analog-to-digital converters) for signal digitizing at >200MHz before further digital processing in the cross-correlators. Power dissipation as well as instrument volume and weight are the most important parameters in space born instruments. Pacific Microchip proposes designing a monolithic array consisting of 20x1-bit ADCs. A serializer will be integrated to reduce the number of outputs from 20 to 1. This will reduce the power per ADC and resolve the problem of wiring congestion where the cross-correlators interface. For further power reduction, Pacific Microchip proposes integrating a novel metastability programming feature into the ADC latches. The clock distribution will also be dramatically simplified. The 2-wire serial I²C (Inter-Integrated Circuit) interface will allow all 1800 ADCs to be calibrated and optimized. Phase I work will provide a complete definition, in silico validation of the product, and a hardware proof of concept. The Phase II program will produce a fieldable product. In order to facilitate the commercialization efforts in Phase III, a low cost commercial radiation-tolerant SiGe HTB technology will be used to fabricate the product.

Primary U.S. Work Locations and Key Partners



Low Power 1-Bit ADC Array with Serial Output, Phase I

Table of Contents

Project Introduction	1
Primary U.S. Work Locations and Key Partners	1
Project Transitions	2
Organizational Responsibility	2
Project Management	2
Technology Maturity (TRL)	2
Technology Areas	3
Target Destinations	3

Low Power 1-Bit ADC Array with Serial Output, Phase I

Completed Technology Project (2010 - 2010)



Organizations Performing Work	Role	Type	Location
Pacific Microchip Corporation	Lead Organization	Industry	Culver City, California
● Jet Propulsion Laboratory(JPL)	Supporting Organization	NASA Center	Pasadena, California

Primary U.S. Work Locations

California

Project Transitions

**January 2010:** Project Start**July 2010:** Closed out

Closeout Documentation:

- Final Summary Chart(<https://techport.nasa.gov/file/140564>)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Pacific Microchip Corporation

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

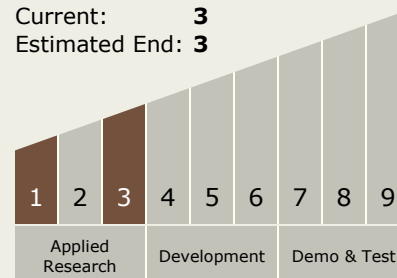
Carlos Torrez

Principal Investigator:

Dalius Baranauskas

Technology Maturity (TRL)

Start: **1**
 Current: **3**
 Estimated End: **3**



Low Power 1-Bit ADC Array with Serial Output, Phase I

Completed Technology Project (2010 - 2010)



Technology Areas

Primary:

- TX08 Sensors and Instruments
 - └ TX08.1 Remote Sensing Instruments/Sensors
 - └ TX08.1.4 Microwave, Millimeter-, and Submillimeter-Waves

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System